

DERWENT-ACC-NO: 2002-563438

DERWENT-WEEK: 200338

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TITLE: Plasma display panel

INVENTOR: AHN, Y J

PATENT-ASSIGNEE: LG ELECTRONICS INC[GLDS]

PRIORITY-DATA: 2000KR-0038273 (July 5, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 366946 B	January 9, 2003	N/A	000	H01J 017/49
KR 2002004407 A	January 16, 2002	N/A	001	H01J 017/49

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR 366946B	N/A	2000KR-0038273	July 5, 2000
KR 366946B	Previous Publ.	KR2002004407	N/A
KR2002004407A	N/A	2000KR-0038273	July 5, 2000

INT-CL (IPC): H01J017/49

ABSTRACTED-PUB-NO: KR2002004407A

BASIC-ABSTRACT:

NOVELTY - A plasma display panel is provided to restrain a rising voltage applied to an address electrode by using a fluorescent layer for exposing a part of lower dielectric layer formed a lower electrode.

DETAILED DESCRIPTION - A scan/sustain electrode(5), a common sustain electrode(8), and a couple of trigger electrode(30,36) are formed on an upper substrate(2). The scan/sustain electrode(5), the common sustain electrode(8), and the trigger electrode couple(30,36) are formed with a transparent electrode(9) and a bus electrode(11), respectively. The trigger electrode

couple(30,36) are aligned between the scan/sustain electrode(5) and the common sustain electrode(8). An upper dielectric layer(10) and a protective layer(12) are laminated on the upper substrate(2). An address electrode(16) is formed on a lower substrate(1). A lower dielectric layer and a barrier(20) are formed on the lower substrate(1). A red, a blue, and a green fluorescent layer(40) are applied on a surface of the lower dielectric layer and a surface of the barrier(20). A groove(A) is formed on the lower dielectric layer. A discharge space(24) is formed between the upper and the lower substrates(2,1) and the barrier(20).

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: PLASMA DISPLAY PANEL

DERWENT-CLASS: V05

EPI-CODES: V05-A01A3B; V05-A01C2;

